INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
CS03-048	
Applicant(s) Yisuo Li	
Filing Date	**Group Art Unit**

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
WL		US 5,970,300		(Buynoski)			
WL		US 6,566,204		(Wang, et al.)			
WL		US 6,599,804		(Bulucea, et al.			
WL		US 4,728,617		Woo, et al			
WL		US 5,729,045		Buynoski			

FOREIGN PATENT DOCUMENTS

	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

EXAMINER	DATE CONSIDERED
	8/17/2005

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INFORMATION DISCLOSURE CITATION *(Use several sheets if necessary)*	Docket Number (Optional) CS03-048	Application Number
	Applicant(s)	
	Filing Date jan 30,2004	Group Art Unit

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*EXAMINER INITIAL		OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*
WLL		Masahi Shima, "<100> Strained-SiGe- channel p-MOSFET with enhanced hole mobility and lower parasitic Resistance", Fujitsu Sci. Tech. J.,39,1, p. 78-83 (June 2003).
WLL		Oldiges, et al., " Molecular Dynamics Simulations of LATID implants into Silicon", found on Website http://beam.helsinki.fi/~knordlun/pub/sispad97.pdf ~3-1-2004 see http://www.acclab.helsinki.fi/~knordlun/pub/
WLL		Brand et al., Intel's 0.25 micron, 2.0V logic process technology, Intel Technology Journal Q3,98, pp. 1-4.

EXAMINER	DATE CONSIDERED
Walter Linh	6/17/2005

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